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# Implementation of WSN node Using Hardware Specialization

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**ABSTRACT : -** *Wireless sensor networks holds space in wide range of application ranging from tracking to monitoring health, environment etc.The power(energy consumption) attribute for WSN requires special attention as WSN has to work unattended for long durations. Till now WSN nodes has been designed using low-power micro-controller. But still its power dissipation is high enough to limit its wide-spread use in new application. We propose an alternate model according to which customized hardware will be designed for each task of an application. The WSN node architecture will be divided into micro-tasks and these micro-tasks will be activated-deactivated by the system monitor which is an FSM (finite state machine).This FSM (hardware monitor) will send all the control signals to the micro-tasks. In our proposed node, system monitor turns-on/off each micro-tasks upon receiving a specific event with the help of power gating technique. This technique is used to reduce both the static and dynamic power and thereby improves the energy efficiency of the computational part of the node. The proposed execution model will be simulated using the Synopsys VCS tool. Design will be synthesized using design compiler and physical implementation using IC compiler. Comparative results will be prepared for power consumption between this proposed architecture and computational part of off-the shelf low-power microcontroller.*

***Keywords:*** *- Customized Hardware, Low -Power Design,WSN Node*

## 1. Introduction

A sensor network is dense network of small nodes sensing the physical world and communicating through wireless links .One of the most important constraints on sensor nodes is the low power consumption requirement. Sensor nodes carry limited, generally irreplaceable, power sources as nodes must be low-cost with reduced scale factors they cannot benefit from significant power-supply sources. Besides, they often have to work unattended for long durations and therefore must survive with either self-harvested (e.g. solar cells) or non-replenishing (e.g. battery) sources of energy.

As far as their design is concerned, WSN nodes have until now been based on low-power MCUs such as MSP430 [1] and ATmega128L [2]. However, power dissipation of current low-power MCUs still remains orders of magnitude too high for many potential applications of WSN.

WSN node consists of four subsystems: a) a computing subsystem having an MCU, b) a communication subsystem having RF transceiver, c) a sensing subsystem having the sensor/actuator interfaces and d) a power Supply subsystem. Among these communication and computation subsystem consume most of the power [3].

## 2. PROPOSED APPROACH

The proposed execution model is made to achieve an ultra low-power system with a simpler task-management strategy that best-suits our micro-task-based system architecture. This architecture is in the form of a minimalistic datapath controlled by a custom finite state machine (FSM) [4].

The monitor is an FSM that will commence its execution when certain starting conditions are met and will run to finish. During each execution state, micro-tasks may be activated or deactivated according to events received by the monitor.

This approach first allows dynamic power savings by reducing hardware complexity. Since the static power contribution will necessarily grow due to the possibly numerous number of hardware tasks implemented on chip, we propose to combine our approach with power gating techniques [5]. The idea consists in supplying power to the hardware controller only when its associated task is to be executed.

## 3. CASE STUDY

As a part of the case study we have design the control tasks running in WSN node in transmit and receive mode. Data transmission by a transmitter node is initiated upon

reception of a wake-up beacon from the desired receiver node. The system level diagram is shown in Fig a.

### 3.1 CONTROL TASKS RUNNING ON A WSN NODE IN TRANSMIT MODE

In our example the communication between the nodes is according to RICER (Receiver Initiated CyclEd Receiver) protocol [6], when transmitter receives the wake-up beacon from receiver, it sends the data by adding the cyclic redundancy code to the data transmitted. After receiving the acknowledgment from the receiver, it will shut down its RF transceiver. The receiver is in any of the four states: Idle, beacon-receive, send-data, acknowledgment-receive.

### 3.2 CONTROL TASKS RUNNING ON A WSN NODE IN RECEIVE MODE.

Our proposed WSN node periodically broadcasts a wake-up beacon to announce the neighbors to initialize a communication. Its receives the data from the transmitter check its CRC. If the received data is error free, acknowledgment signal is sent to transmitter. Depending upon the value of the received data, signal is generated to switch on/off the device. The transmitter is in either of five states: idle, send-beacon, receive-data, send-acknowledgement, device-on/off.

### 3.3 SYSTEM MONITOR

The SM works like finite state machine .It turns-on/off each micro-task upon receiving a specific event or a set of events with the help of power-gating technique. It is implemented as a combinational FSM and a set of status registers and event registers [7]. The event registers save the activation status of the micro-tasks and are controlled by the FSM and status register contains the states of SM. The state diagram is shown in Fig b

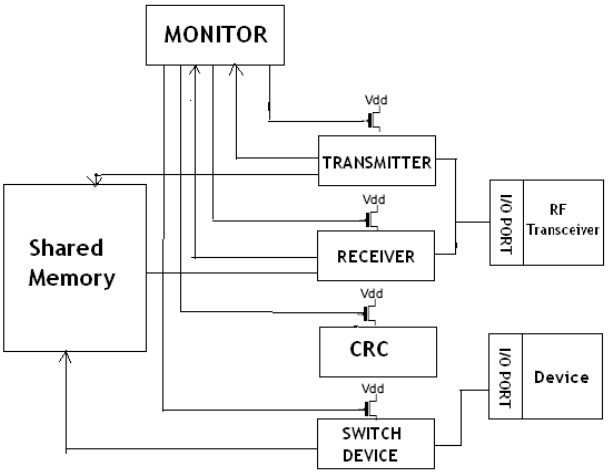


Fig. a

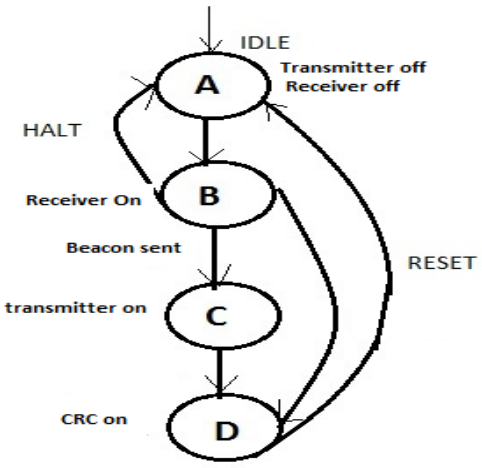


Fig. b

## 4. SYNOPSYS LOW POWER FLOW

The flow starts with the register-transfer level (RTL) description of the logic of the design, together with a separate UPF (Unified Power Format) description of the power intent of the design. The RTL and UPF descriptions are contained in separate files so that they can be maintained and modified separately.

Design Compiler [8] reads in the RTL logic and original UPF power intent descriptions, and based on their contents, synthesizes a gate-level netlist and an update the original UPF file.

IC Compiler reads in the gate-level netlist and power description files, and based on the file contents, performs physical implementation (placement and routing), producing a modified gate-level netlist, a complete power and ground (PG) netlist, and an updated UPF.

The VCS simulator and MVSIM multivoltage simulation tool can be used for functional verification of the design with multivoltage features at several different stages of the flow: at the RTL level before synthesis, at the gate level after synthesis with power-related cells added, and after placement and routing with the power switches added.

## 6. CONCLUSION

In this paper, we have proposed, a novel approach for ultra low-power implementation of control-oriented application tasks of a WSN node. Our approach is based on power-gated micro-tasks that are implemented as specialized hardware blocks. The synthesis results obtained for the micro-tasks of the case study show that compared with a software implementation such as the MSP430 microcontroller, power reductions of one to two orders of magnitude are possible.

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